What is Claimed is:

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- 1. An auto refresh control circuit of a semiconductor memory device, comprising:
- 5 a command decoder for generating an auto refresh signal performing an auto refresh operation;
 - a wordline control means for activating wordlines when the auto refresh signal is activated, and for precharging the wordlines when an auto refresh operation is finished; and
 - a buffer control means for inactivating the input buffers when the auto refresh signal is activated or a power down signal is activated, and for activating the input buffers when a signal detecting the end time of an auto refresh is activated,

wherein when the input buffers are inactivated, the command decoder and input latches are inactivated.

- 2. The circuit according to claim 1, wherein the 20 signal detecting the end time of the auto refresh is a signal for activating the wordlines when the auto refresh signal is activated, the signal delayed during the auto refresh operation.
- 25 3. The circuit according to claim 1, wherein the command decoder and input latches are controlled by a clock signal outputted from a clock buffer among the input buffers.

4. The circuit according to claim 1, wherein the signal detecting the end time of the auto refresh is a precharge signal for precharging the wordlines.

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- 5. The circuit according to claim 1, wherein the buffer control means includes:
- a pull-up means for pulling up an output terminal when the auto refresh signal is activated; and
- 10 a pull-down means for pulling down the output terminal when the signal detecting the end time of the auto refresh is activated.
- 6. The circuit according to claim 5, wherein the buffer control means further includes a latch means for maintaining a potential of the output terminal.
- The circuit according to claim 6, wherein the buffer control means further includes a logic means for
 inactivating the input buffers irrespective of the potential of the output terminal, when the power down signal is activated.